

INFORMATION DISCLOSURE CITATION

Atty. Docket No.	04329.2343-02	Div. of Appln. No.	10/200,446 /0810837
Applicant	Atsushi YAGISHITA et al.		
Filing Date	Herewith	Prior Group:	2823

U.S. PATENT DOCUMENTS						
Examiner Initial*	Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
DM	4,996,574	02/1991	Shirasaki			
VM	6,165,828	09/1998	Forbes et al.			
VM	6,177,299 B1	01/1998	Hsu et al.			

FOREIGN PATENT DOCUMENTS						
	Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No
VM	10-242477	09/1998	Japan			
VM	09162302 A	06/1997	Japan			
VM	03205869 A	09/1991	Japan			
VM	CN 1186346A	07/1998	People's Republic of China			
VM	05343687A	12/1993	Japan			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
VM	Assaderaghi, F., "Dynamic Threshold-Voltage MOSFET (DTMOS) for Ultra-Low Voltage VLSI," IEEE Trans. Electron Devices, Vol. 44, pp. 414-422, March 1997
VM	Wong et al., "A 1V CMOS Digital Circuits With Double-Gate-Driven MOSFET," IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE DIGEST OF TECHNICAL PAPERS, February 1997, pp. 292, 293, and 473

Examiner	Date Considered
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	
Form PTO 1449	Patent and Trademark Office - U.S. Department of Commerce